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(54) RADAR VIDEO PROCESSORS

(71) We, SPERRY RAND CORPORATION, a Corporation organised and existing under the laws of the State of Delaware, United States of America, of 1290 Avenue of the Americas, New York, New York 10019, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to radar video processors wherein a detection threshold may be adjusted in accordance with the background noise and interference.

A number of detection techniques for radar, sonar and other detection systems have been proposed in which the deetction threshold is automatically adjusted in accordance with variations in background noise and interference. These systems include rank sum, rank quantization and unknown level detection. A rank sum detector passes a video signal through a tapped delay line, whereon the mean signal amplitude, determined over a range cell interval at each tap, represents the return signal for a given range cell and on which the presence of a target is sought in the range cell represented by the central tap. The rank of the central tap is determined by comparing the mean signal amplitude at the central tap to the mean signal amplitude at each of the other taps. The rank of the central tap is the number of range cells, in a given group of range cells, wherein the mean amplitude is less than the mean amplitude in the range cell represented by the central tap. A target is declared, for the range cell represented by the central tap, when the sum of the ranks obtained after several range sweeps exceeds a specified threshold.

The rank quantization detector, like the rank sum detector, compares the signal level at the centre tap of a tapped delay line with the signal levels at all the other taps. However, instead of obtaining a rank sum after a number of transmitted pulses and comparing the rank sum to a given threshold, the rank quantization detector compares the rank obtained after each transmitted pulse with a specified threshold, sums the number of ranks exceeding the threshold after a number of transmitted pulses and compares the sum with a second threshold to determine the presence of a target.

The unknown level detector also employs a tapped delay line whereon the range cell represented by the central tap is the one of interest. In this detector the square of the mean of the return signal, determined over a range cell interval at the central tap, is compared with the average of the sum of the squares of the means of the return signals at all the other taps and a hit or a miss is declared, after each transmitted pulse, when the ratio of the square of the mean signal at the centre tap to the average of the squares of the mean signals at all the other taps exceeds a specified threshold. As in the rank quantization detector, a target report is given when the sum of the hits obtained after a number of transmitted pulses exceeds a given threshold.

Known systems provide approximately the same levels of performance and require complex circuitry and an appreciable number of components to achieve a desired probability of target detection. The present invention provides a radar video processor which can be made adjustable to background noise and interference and which realises a significant reduction in complexity and the number of required components while matching or exceeding the levels of performance achieved by known systems.

According to the invention a radar video processor comprises a first input terminal for receiving sets of primary sequential signals, each of a predetermined time duration, a primary intergrator, coupled to the first input terminal, for integrating each of the primary signals over the predetermined time duration, thereby providing an integrated value for each of the primary signals, and a comparator, coupled to the primary integrator, wherein the integrated value of one of the primary sequential signals is compared with the integrated values of primary signals adjacent thereto, the comparison providing data

which specifies whether the ratios of the integrated value of each of the primary sequential signals to the integrated values of the adjacent primary signals are greater than a predetermined value.

In the preferred form of the radar video processor, disclosed in greater detail hereinafter, squared video signals are coupled to an integrator wherein the squared video signal contained within each of three successive range cells is integrated, thereby determining the energy contained therein. The terms, energy level and integrated squared video are used interchangeably hereafter. The energy levels in each range cell are couple to a comparator wherein the energy contained within the central range cell is compared with the energy contained within the two adjacent range cells. When this comparison reveals ratios of the energy in the central range cell to the energy in each of the two adjacent range cells. When this comparison reveals ratios of the energy in the central range cell to the energy in each of the two adjacent range cells that are both greater than a specified value, the output signal from the comparator provides a positive indication of an echo signal or a target contained within the central range cell.

To prevent the loss of a target that straddles two range cells the integrator also integrates squared video that is delayed for a time equal to one-half of a range cell. The integrated delayed square video is processed by the comparator in the same manner as the integrated undelayed squared video and combined therewith to provide a single output which is attributed to the central range cell of the undelayed video.

The probability of a target report due to impulse interference or noise is minimised by coupling the output signal from the comparator to a M of N detector wherein the positive indication provided by the output signals of the comparator for a given range cell is summed over a number of range sweeps. Whn this sum achieves a specified number, a target is indicated. The output of the M of N detector for each range cell is a one or a zero depending upon whether the energy in a given range cell has or has not met both detection criteria. This information is coupled to a trailing edge detector wherein, for data reduction purposes, the existence of a target in a given range cell is not reported until after the M of N detector output, for the give range cell provides one or more ones followed by a zero.

A radar video processor according to the invention will now be described, by way of example, with reference to the accompanying drawings, in which:—

Figs. 1*a* and 1*b* together represent a block diagram of the radar video detector.

Fig. 2 is a schematic diagram, partially in block form, of a comparator suitable for use in the video detector of Figs. 1*a* and 1*b*, and

Fig. 3 is a block diagram of a shift register suitable for use in the M of N detector of Fig. 1*b*.

Figs. 1*a* and 1*b* show a block diagram of the preferred embodiment of the radar video processor which comprises an integrator 11, a comparator 12, a land elimination unit 13, a M of N deetctor 14, and a trailing edge detector 15. The integrator 11 comprises a primary switch 16, a secondary switch 17, a plurality of operational amplifiers which are designated primary integrators 20, 21 and 22, a plurality of operational amplifiers which are designated secondary integrators 23, 24 and 25, a primary integrator reset unit 26 and a secondary integrator reset unit 27.

The primary switch 16 has one input terminal 16*a* and three output terminals 16*b*, 16*c* and 16*d*. The input terminal 16*a* receives squared radar video from a video squaring unit (not shown) which squares the radar detected video in each range cell contained in a range sweep, thus forming sets of sequential video signals. Each set corresponds to a range sweep, with the number of elements (squared video signals) contained therein determined by the number of range cells within a range sweep. These sets of signals are cyclically coupled to terminals 30*a*, 31*a* and 32*a* of the primary integrators 20, 21 and 22, respectively, in which the squared video is integrated. While the second and third primary integrators 21 and 22 are holding the integrated values obtained from the integration of the second and third range cells, respectively, the primary switch 16 is clocked to couple squared video of the fourth range cell with the first primary integrator 20. During the first half of the interval in which the primary integrator 20 integrates the squared video of the fourth range cell, the comparator 12 is clocked to compare the integrated squared video of range cells 2 and 3 which are held by the second and third primary integrators 21 and 22.

The comparator 12 comprises: a primary detector 33, a comparator logic unit 34, and a secondary detector 35. The primary detector 33 contains three inputs, a first input terminal 36 is coupled to an output terminal 37 of the first primary integrator 20, a second input terminal 38 is coupled to an output terminal 41 of the second primary integrator 21 and a third input terminal 42 is coupled to an output terminal 43 of the third primary integrator 22; and six output terminals 38*a* to 38*f* which are respectively coupled to six input terminals 39*a* to 39*f* of the comparator logic unit 34. The secondary detector 35 contains: three input terminals, a first input terminal 44 is coupled to an output terminal 45 of the first secondary integrator 23, a second input terminal 46 is coupled to an

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output terminal 47 of the second secondary integrator 24, and a third input terminal 48 is coupled to an output termianl 49 of the third secondary integrator 25; and six output terminals 50*a* to 50*f* which are respectively coupled to six input terminals 51*a* to 51*f* of the comparator logic unit 34.

The primary detector 33, the comparator logic unit 34 and the secondary detector 35 may be as shown in the schematic diagram of Fig. 2. The primary detector 33 comprises six ratio detectors 33*a* to 33*f*, and six flip-flops 52*a* to 52*f*. The output terminal 37 of the first primary integrator 20 is coupled to the ratio detectors 33*a*, 33*b*, 33*c* and 33*e* while the output terminal 41 of the second primary integrator 21 is coupled to the ratio detectors 33*a*, 33*c*, 33*d* and 33*f* and the output terminal 43 of the third primary integrator 22 is coupled to the ratio detectors 33*b*, 33*d*, 33*e* and 33*f*. The output terminals of each of the ratio detectors 33*a* to 33*f* are coupled to the input terminals of the flip-flops 52*a* to 52*f*, respectively, while the output terminals of the flip-flops 52*a* to 52*f*, which are the primary detector output terminals 38*a* to 38*f*, are coupled to the input terminals 39*a* to 39*f*, respectively, of the comparator logic unit 34, wherein the terminals 39*a* to 39*b* are input terminals to a NAND gate 53*a*, the terminals 39*c* and 39*d* are input terminals to a NAND gate 53*b* and the terminals 39*e* and 39*f* are input terminals to a NAND gate 53*c*.

The secondary detector 35 comprises six ratio detectors 35*a* to 35*f* and six flip-flops 54*a* to 54*f*. The output terminal 45 of the first secondary integrator 23 is coupled to the ratio detectors 35*a*, 35*b*, 35*c* and 35*e* while the output terminal 47 of the secondary integrator 24 is coupled to the ratio detectors 35*a*, 35*c*, 35*d* and 35*f*, and the output terminal 49 of the third secondary integrator 25 is coupled to the ratio detectors 35*b*, 35*d*, 35*e* and 35*f*. The output terminals of each of the ratio detectors 35*a* to 35*f* are coupled to the input terminals of flip-flops 54*a* to 54*f*, respectively, while the output terminals of the flip-flops 54*a* to 54*f*, which are the secondary detector output terminals 50*a* to 50*f*, are coupled to the input terminals 51*a* to 51*f*, respectively, of the comparator logic unit 34, wherein terminals 51*a* and 51*b* are input terminals to a NAND gate 55*a*, the terminals 51*c* and 51*d* are input terminals to a NAND gate 55*b* and the terminals 51*e* and 51*f* are input terminals to a NAND gate 55*c*.

The comparator logic unit 34 further includes NAND gates 56*a*, 56*b* and 56*c* wherein a first input terminal of the NAND gate 56*a* is coupled to the output terminal of the NAND gate 53*a* and a second input terminal to the NAND gate 56*a* is coupled to the output terminal of the NAND gate 55*a*, while a first input terminal to the NAND gate 56*b* is coupled to the output terminal of the NAND gate 53*b* and a second input terminal to the NAND gate 56*b* is coupled to the output terminal of NAND gate 55*b*, and the input terminal to the NAND gate 56*c* is coupled to the output terminals of the NAND gates 53*c* and 55*c*. The output terminal of the NAND gate 56*a* is coupled to one input of an AND gate 65*a*, the other input of which is coupled to the output terminal of the NAND gate 53*c*. A first input terminal to an AND gate 65*b* is coupled to the output termnial of the NAND gate 56*b* and a second input terminal is coupled to the output terminal of the NAND gate 53*a*, while a first input terminal to an AND gate 65*c* is coupled to the output terminal of the NAND gate 56*c* and a second input terminal is coupled to the output terminal of the NAND gate 53*b*. The output terminals of the AND gates 65*a*, 65*b* and 65*c* are coupled respectively to one input of NAND gates 76*a*, 76*b* and 76*c*, and second inputs to the NAND gates 76*a*, 76*b* and 76*c* are coupled to the output terminals 80*a*, 80*b* and 80*c* respectively of the primary integrator reset unit 26 in Fig. 1*a*. The output of the NAND gate 76*a* is coupled to a first input terminal of a NAND gate 78, while the output terminals of the NAND gates 76*b* and 76*c* are coupled to a second and third input terminal, respectively. The output terminal of the NAND gate 78 is coupled to one input terminal of a AND gate 81, the other input of which is coupled to the output terminal 82 of the land elimination unit 13 of Fig. 1*a*.

With the primary integrators 21 and 22 holding the energy levels of the second and third range cells, respectively, the primary switch 16 is clocked to couple the squared video of the fourth range cell to the input terminal 30*a* of the first primary integrator 20, and the d.c. levels held in the integrators 21 and 22 are compared in the ratio detectors 33*d* and 33*f*. When the ratio of the d.c. level held in the second primary integrator 21 to the d.c. level held in the third primary integrator 22 exceeds a specified value, a high level signal is coupled from the ratio detector 33*d* to the input terminal of the flip-flop 52*d* and a low level signal is coupled from the ratio detector 33*f* to the input terminal of the flip-flop 52*f*. When the reciprocal of this ratio exceeds the specified value, the high and low level signals are reversed at the inputs of the flip-flops 52*d* and 52*f*. Low level signals are coupled to both inputs when neither ratio exceeds the specified value.

During the first half of the interval in which the primary integrator 20 integrates the squared video of the fourth range cell, the signal levels at the input terminals of the flip-flops 52*d* and 52*f* are strobed into the flip-flops 52*d* and 52*f*, with the level in the

flip-flop 52*d* being coupled to the input terminal 39*d* of the NAND gate 53*b* and the level in flip-flop 52*f* being coupled to the input terminal 39*f* of the NAND gate 53*c*. During the second half of the interval in which the first primary integrator 20, Fig. 1*a* integrates the squared video of range cell 4, the second primary integrator 21 is reset by a signal from the output terminal 80*b*, of the primary integrator reset unit 26, which is coupled to a terminal 31*b* of the second primary integrator 21 and the primary switch 16 is clocked to couple the squared video of range cell five to the input terminal 31*a* of the second primary integrator 21.

At the conclusion of the interval in which the primary integrator 20 integrates the squared video in range cell 4, the value then held is coupled to the ratio detectors 33*a*, 33*b*, 33*c* and 33*e* and the second primary integrator 21 commences to integrate the squared video of range cell five. The d.c. levels now held in the third primary integrator 22 and in the first primary integrator 20 are comprade in ratio detectors 33*b* and 33*e*. When the ratio of the d.c. level in the first primary integrator 20, to the d.c. level held in the third primary integrator 22 exceeds the specified value, a high level signal is coupled from the ratio detector 33*b* to the input terminal of the flip-flop 52*b* and a low level signal is coupled from the ratio detector 33*e* to the input terminal of the flip-flop 52*e*. If the reciprocal of this ratio exceeds the specified value, the level of the signals coupled to the flip-flops 52*b* and 52*e* are reversed.

During the second half of the interval in which the second primary integrator 21 integrates the squared video of range cell five, the signal levels at the input terminals of the flip-flops 52*b* and 52*e* are strobed into the flip-flops 52*b* and 52*e*, with the signal level in the flip-flop 52*b* being coupled to the input terminal 39*b* of the NAND gate 53*a* and the signal level in the flip-flop 52*e* being coupled to the input terminal 39*e* of the NAND gate 53*c*. At this time signals representing the four possible ratios of the energy contained in range cell three to that contained in range cells two and four exist at four of the six input terminals 39*b*, 39*d*, 39*e* and 39*f* of the NAND gates 53*a*, 53*b* and 53*c*. When the flip-flops 52*e* and 52*f* are both at a high signal level state, it indicates that the ratios of the integrated value obtained by the third primary integrator 22 for the squared video of range cell three to the integrator 22 for the squared video of range cell three to the integrated values obtained by the first primary integrator 20 for the squared video of range cell four and the second primary integrator 21 for the squared video of range cell two, exceed the specified value.

Thus, high level signals are coupled to the input terminals 39*e* and 39*f* of NAND gate 53*c* and low level signals are coupled to the input terminal 39*b* of NAND gate 53*a* and to the input terminal 39*d* of the NAND gate 53*b*, resulting in high level signals at the output terminals of the NAND gates 53*a* and 53*b* and a low level signal at the output terminal of the NAND gate 53*c*. The high level signal at the output of the NAND gate 53*a* is coupled to one input terminal of the NAND gate 56*a*, the high level signal at the output of the NAND gate 53*b* is coupled to one input terminal of the NAND gate 56*b* and the low level signal at the output of the NAND gate 53*c* is coupled to one input terminal of the NAND gate 56*c*, while the second input terminals of the NAND gates 56*a*, 56*b* and 56*c* are coupled to the output terminals of the NAND gates 55*a*, 55*b* and 55*c*, respectively. The input terminals 51*a* to 51*f* of the NAND gates 55*a*, 55*b* and 55*c* are coupled to the output terminals 50*a* to 50*f* of the secondary detector 35, the purpose of which will be explained subsequently.

It is now assumed that low level signals exist at the output terminals of the NAND gates 55*a*, 55*b* and 55*c*. As a consequence thereof, high level signals are established at the output terminals of the NAND gates 56*a*, 56*b* and 56*c*. These high level signals are coupled respectively to input terminals of the AND gates 65*a*, 65*b* and 65*c*. The low level signal at the output terminal of the NAND gate 53*c* is coupled to a second input terminal of the AND gate 65*a*, the high level signal at the output terminal of the NAND gate 53*a* is coupled to a second input terminal of the AND gate 65*b* and the high level signal at the output terminal of the NAND gate 53*b* is coupled to a second input terminal of the AND gate 65*c*.

As a result of the signal levels that exist at the input terminals of the AND gates 65*a*, 65*b* and 65*c*, a low level signal exists at the output terminal of the AND gate 65*a* and high level signals exist at the output terminals of the AND gates 65*b* and 65*c*. These signals are coupled to respective input terminals of the NAND gates 76*a*, 76*b* and 76*c*. The second input terminals of the NAND gates 76*a*, 76*b* and 76*c* are coupled to terminals 80*a*, 80*b* and 80*c*, respectively, of the primary integrator reset unit 26 in Fig. 1 whereby the reset waveform for the first primary integrator 20 is coupled to the NAND gate 76*a*, the reset waveform for the third primary integrator is coupled to the NAND gate 76*c*.

During the second half of the time interval in which the primary integrator 21 integrates the squared video contained in range cell five, a reset pulse from the terminal 80*c* of the primary reset unit 26 is coupled to the third primary integrator 22 and is also

coupled to the second input terminal of the NAND gate 76c. The second input terminal of the NAND gate 76a remains at a low level signal until a reset pulse is applied to the first primary integrator 20, and the second input terminal of the NAND gate 76b remains at a low signal level until a reset pulse is applied to the second primary integrator 21.

The signal levels at the output terminals of the NAND gates 76a, 76b and 76c are coupled to the input terminals 79a, 79b and 79c, respectively, of the NAND gate 78, the output terminal of which as a consequence of the two high level signals and the one low level signal at the input terminals provides a high level signal signifying the presence of a target in range cell 3. This high level signal is coupled to an input terminal 81a of the AND gate 81, the input terminal 81b of which is coupled to the output terminal 82 of the land elimination unit 13 in Fig. 1a.

In a marine radar, it is often desirable to blank target indications of large masses. To accomplish this, the land elimination unit 13 is employed. Referring now to Fig. 1a, a first input terminal 84c of the land elimination unit 13 is coupled to the output terminal 37 of the first primary integrator 20, a second input terminal 84b is coupled to the output terminal 41 of the second primary integrator 21 and a third input terminal 84a is coupled to the output terminal 43 of the third primary integrator 22. When the signal level at each of the output terminals 37, 41 and 43 exceeds a predetermined reference level, a low level signal appears at the output terminal 82 of the land elimination unit 13. This low level signal is coupled to terminal 81b of the AND gate 81 of Fig. 2, causing a low level signal to appear at the output terminal 85 thereof, thus blanking any target indication.

When at least one of the signal levels at the output terminals of the integrators 20, 21 and 22 does not exceed the reference level, a high level signal appears at the output terminal 82 of the land elimination unit 13 which is coupled to the second input terminal 81b of the AND gate 81, permitting the output terminal thereof to exhibit the signal level that corresponds to the signal level at the first input terminal 81a of the AND gate 81.

In Fig. 1a, the combination of the secondary switch 17, the secondary integrator reset unit 27 and the secondary integrators 23, 24 and 25 in the integrator 11, and the secondary detector 35 in the comparator 12 are included to prevent a loss of target detection when a target straddles two range cells. The squared video signal is delayed in time, the delay being equal to one-half the time interval of a range cell, and is coupled to the input terminal 17a of the secondary switch 17 which operates in the same manner as the primary switch 16, cyclically coupling the delayed squared video to secondary integrators 23, 24 and 25. Each integrator 23, 24 or 25 is cleared prior to the coupling of the squared video of the next delayed range cell to be integrated by that integrator, by signals from secondary integrator reset unit 27 that are coupled to the terminals 23b, 24b and 25b of secondary intergrators 23, 24 and 25. The signal levels at the output terminals 45, 47 and 49 of the integrators 23, 24 and 25 are coupled to the input terminals 44, 46 and 48, respectively, of the secondary deetctor 35 which is identical to the primary detector 33, with the high and low level signals at the output terminals 50a to 50f of the secondary detector 35 being coupled to the input terminals 51a to 51f, respectively, of the comparator logic unit 34.

When a target is located half in range cell 2 and half in range cell 3, the primary ratio detector provides low level signals which are coupled to the input terminals 39b, 39d, 39e and 39f of the NAND gates 53a, 53b and 53c causing high level signals to be coupled to one terminal of each NAND gate 56a, 56b and 56c and to one terminal of each AND gate 65a, 65b and 65c. Since the target straddles range cells two and three, it appears completely in the delayed range cell three, causing the secondary ratio detector 35 to couple low level signals to the input terminals 51b and 51d of the NAND gates 55a and 55b respectively, and high level signals to the input terminals 51e and 51f of the NAND gate 55c. This results in the coupling of high level signals to one terminal of the NAND gates 56a and 56b and a low level signal to the NAND gate 56c. The signals at the output terminals of the NAND gates 56a, 56b and 56c and NAND gates 53a, 53b and 53c, which are coupled to the input terminals of the AND gates 65a, 65b and 65c, establish low level signals at the output terminals of the AND gates 65a and 65b and a high level signal at the output of the AND gate 65c. Thus, high level signals exist at the output terminals of the NAND gates 76a and 76b. A high level signal also exists at the output terminal of the NAND gate 76c until the reset signal from terminal 80c of the primary integrator reset unit 26 goes high and resets the primary integrator 22. At this time the signal at the output terminal of the NAND gate 76c is switched to a low level resulting in a high level signal or target indication at the output terminal of the NAND gate 78.

Thus logic unit 34 performs a correlation of the output signals from the primary and secondary detectors 33 and 35, as a result of which a target is indicated in primary range cell three when the ratios of the energy in the corresponding range cell of the delayed video signal to the energy in the range cells

adjacent thereto, each exceed the specified value.

Referring again to Fig. 1*a*, the output terminal 85 of the comparator logic unit 34 is coupled to the M of N detector 14, which comprises a shift register unit 92, a PRF (pulse repetition frequency) detector 93, an adder 94, and three NAND gates 95, 96 and 97. Input signals to the M of N detector are coupled via a line 91 to the shift register unit 92, which may comprise seven serially coupled shift registers 92*a* to 92*g* as shown in Fig. 3. Each of the output terminals of the seven shift registers 92*a* to 92*g* is coupled to one of seven input terminals of the adder 94 via lines 99*a* to 99*g*. The number of operating shift registers of the shift register unit 92 is adapted to the pulse repetition frequency (PRF) of a PRF generator, not shown, by the PRF deetctor 93 which provides a high or a low level signal to the recirculate control terminal of the shift register 92*d* via a line 98. A high level signal from the PRF detector 93, indicating a PRF equal to 500 pulses per second, places the shift register 92*d* in the recirculate mode preventing the entry of data therein. A low level signal at the output terminal of the PRF detector 93 indicating that the PRF is above 500 cycles per second, places the shift register 92*d* in the operating mode, thus making all seven shift registers available for data storage.

With a radar operating PRF of 500 pulses per second, output data from the comparator logic unit 34, which consists of a series of ones and zeroes representing a target indication or no target indication, are sequentially strobed into the three operating shift registers 92*a*, 92*b* and 92*c*. At the completion of three range sweeps, the target data for each range cell within the range sweep is contained in the three shift registers in reverse order. That is, the data from the first range cell in the first range sweep is containd in the last stage of the shift register 92*c*, the data from the first range cell of the second range sweep is contained in the last stage of the shift register 92*b* and the data from the first range cell of the third range sweep is contained in the last stage of shift register 92*a*.

The data in each of the last stages of the shift registers 92*a*, 92*b* and 92*c* is sampled in the following manner. When the data from the first range cell of the fourth range sweep is strobed into the first stage of the shift register 92*a*, the data from the first range cell of the third range sweep is strobed out of the shift register 92*a* and coupled to the adder 94 via the line 99*a* and to the first stage of the shift register 92*b*. This data in turn strobes out the first range cell of the second range sweep which is also coupled to the adder 94 via the line 99*b* and is also strobed into the first stage of the shift register 92*c*. This data in turn strobes out the first range cell of the first range sweep which is coupled to the adder 94 via the line 99*c*. Since the shift register 92*d* is in the recirculate mode, no data can be entered and the sequence terminates. In this manner, the data stored for each range cell, within a range sweep, has been sequentially sampled for target indications by the adder 94.

The adder 94 sums the ones (target indications), coupled from the shift register 92 via the lines 92*a*, 92*b* and 92*c*, and provides a high level signal at a terminal 94*a*, if this sum is two or more; otherwise, a low level signal will be present at the terminal 94*a*. This signal is coupled to a first input terminal of the NAND gate 95, a second input terminal of which is coupled to a terminal 93*a* on the PRF detector 93. With two high level signals at the input terminals of the NAND gate 95, one representing a PRF of 500 pulses per second, the other signifying that a given range cell has a target indication for at least two of three consecutive range sweeps, a low level signal at the output terminal results. This low level signal is coupled to a first input of the NAND gate 97.

A terminal 94*b*, at which a high level signal would appear when all seven shift registers are in the operate mode and the data for a given range cell exhibits a target indication for at least four of seven consecutive range sweeps, is at a low signal level due to the cut-off of data entry at the shift register 92*d*. This low level signal is coupled to a first terminal of the NAND gate 96, a second terminal of which is coupled to a terminal 93*b* of the PRF detector 93 at which a low level signal exists when a PRF greater 500 pulses per second is detected, and a high level signal exists when a PRF greater than 500 pps is detected. The low level signals at the input terminals of the NAND gate 96 result in a high level signal at the output terminal which is coupled to a second input of the NAND gate 97. The high and low level signals at the input terminals of the NAND gate 97 result in a high level signal at the output terminal. This signal is coupled to the input terminal 15*a* of the trailing edge detector 15 which comprises, a shift register 103, an inverter 104, and an AND gate 105. An input terminal of the inverter 104 and an input terminal of the shift register 103 are coupled to the input terminal 15*a* of the trailing edge detector 15. When the data at the terminal 15*a* is strobed into the shift register 103, the previously stored data for this range cell is strobed out of the shift register 103 and coupled to a first input of the AND gate 105. The data at the terminal 15*a* is also coupled to the inverter 104, the output of which is coupled

to a second input terminal of the AND gate 105, to which a strobe clock signal is coupled to a third input terminal.

In this manner, the previous range cell data is compared with the present range cell data to determine whether the radar sweep has passd the target. Consider that the previous data has indicated a target, a one or high level signal being strobed out of the shift register 103, and that the present data does not indicate a target, that is, the signal level at the terminal 15*a* is a zero or low level signal. The low level signal at the terminal 15*a* is inverted by the inverter 104, thereby coupling a high level signal to the second input of the AND gate 105. At this time, a high level signal from a strobe clock also exists at the third input terminal to the AND gate 105. Since three high level signals exist at the three input terminals of the AND gate 105, a high level signal exists at the output terminal and a target is reported at an output terminal 106. If the previous range cell data did not indicate a target or the present range cell data did indicate a target, a low level signal would exist at the output terminal of the AND gate 105 and a target would not be reported.

WHAT WE CLAIM IS:—

1. A radar video processor comprising a first input terminal for receiving sets of primary sequential signals, each of a predetermined time duration, a primary integrator, coupled to the first input terminal, for integrating each of the primary signals over the predetermined time duration, thereby providing an integrated value for each of the primary signals, and a comparator, coupled to the primary integrator, wherein the integrated value of one of the primary sequential signals is compared with the integrated values of primary signals adjacent thereto, the comparison providing data which specifies whether the ratios of the integrated value of each of the primary sequential signals to the integrated values of the adjacent primary signals are greater than a predetermined value.

2. A radar video processor according to claim 1, wherein the primary integrator comprises a plurality of primary operational amplifiers wherein each of the primary sequential signals is integrated over the predetermined time duration and held for the comparison thereat; a primary switch, coupled between the first input terminal and the plurality of primary operational amplifiers, for successively and cyclically coupling the primary sequential signals at the first input terminal to the plurality of primary operational amplifiers, and a primary integrator reset, coupled to the plurality of operational amplifiers, to provide signals to clear each of the plurality of primary operational amplifiers in a sequential manner so that each of the primary operational amplifiers is cleared immediately prior to being coupled to the first input terminal by the primary switch, whereby one of the primary operational amplifiers integrates one of the primary sequential signals over the time duration of the primary signal and holds the integrated value for a period determined by the primary switch and the primary integrator reset.

3. A radar video processor according to claim 1 or 2 wherein the comparator comprises a primary detector, coupled to the primary integrator, for providing a plurality of output signals which indicate whether the ratio of the integrated value of each of the primary sequential signals to the integrated value of the signals adjacent thereto exceeds the predetermined value, and logic means, including an output terminal, for determining, from the plurality of output signals of the primary detector, each of the primary sequential signals for which the integrated value exceeds the integrated values for signals adjacent thereto by the predetermined ratio.

4. A radar video processor according to claim 3 and further including a second input sequential input signals each of a predetermined time duration, a secondary integrator, coupled to the second input terminal, for integrating each of the secondary signals over the predetermined time duration, thereby providing an integrated value for each of the secondary signals, and wherein the comparator further includes a secondary detector, coupled to the secondary integrator, for providing a plurality of output signals representative of the ratios of the integrated value of each of the secondary sequential signals to the integrated values of the signals adjacent thereto; the plurality of output signals being coupled to the logic means, for correlating the plurality of output signals from the primary and secondary detectors to provide an output signal for each of the primary ratios of the integrated values for each of the primary signals or its corresponding secondary signal exceed the predetermined value.

5. A radar video processor according to all of the preceding claims wherein the secondary integrator includes a plurality of secondary operational amplifiers for integrating each of the secondary sequential signals over the predetermined time duration and holding the value so obtained, a secondary switch coupled between the second input terminal and the plurality of secondary operational amplifiers, for successively and cyclically coupling the secondary sequential signals at the second input terminal to the plurality of secondary operational amplifiers, and a secondary integrator reset, coupled to the

plurality of secondary operational amplifiers, to provide signals for clearing each of the plurality of secondary operational amplifiers in a sequential manner so that each of the secondary operational amplifiers is cleared immediately prior to being coupled to the second input terminal by the secondary switch, whereby one of the secondary operational amplifiers integrates one of the secondary sequential signals over the time duration of the secondary signal and holds the integrated value for a period determined by the secondary switch and the secondary integrator reset.

6. A radar video processor according to claim 3, 4 and 5 and further including means for coupling the signals from said primary integrator reset to the logic means, whereby the comparison data is provided at the output terminal of the logic means during the receipt of the signal from the primary integrator reset.

7. A radar video processor according to any of the preceding claims and further including a plurality of storage devices, coupled to the comparator, for storing the data from the comparator, each of the storage devices containing a plurality of storage cells, each storage cell being for storing data for one of the integrated value comparisons, the storage being accomplished in the same sequential order as the sequential input signals for which the integrated value comparisons are performed, and a sampling device, coupled to the plurality of storage devices, for sampling one of the storage cells in each of a specified number of the storage devices, each of the sampled storage cells containing data of the integrated value comparison for input signals in the same relative position of the sequential input signals in each of a number of the sets of sequential input signals, the number of the sets being equal in number to the specified number of storage devices, to determine if a predetermined quantity of the storage cells contain data specifying that the ratios of the integrated values of the signals in the same relative position of the sequential input signals exceed the predetermined value.

8. A radar video processor according to claim 7, wherein the sampling device contains means for selecting the specified number from a plurality of available specified numbers and the predetermined quantity from a plurality of available predetermined quantities.

9. A radar video processor according to claim 7 or 8 and further including means, coupled to the sampling device for providing a positive output when the sampling device determines that the specified number of sets of sequential input signals does not provide the predetermined quantity of storage cells that contain data indicating that the number of ratios of integrated values exceed the predetermined value after the sampling device has determined that the predetermined quantity of storage cells contain data indicating that the number of ratios of integrated values exceed the predetermined value for at least the previous specified number of sets of sequential input signals.

10. A radar video processor according to all the preceding claims and further including means, coupled to the primary integrator and the comparator for inhibiting data from the comparator when the integrated value for each of the input signals exceeds a predetermined reference value.

11. A radar video processor constructed and arranged substantially as herein particularly described with reference to the accompanying drawings.

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1509464 COMPLETE SPECIFICATION
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Sheet 1

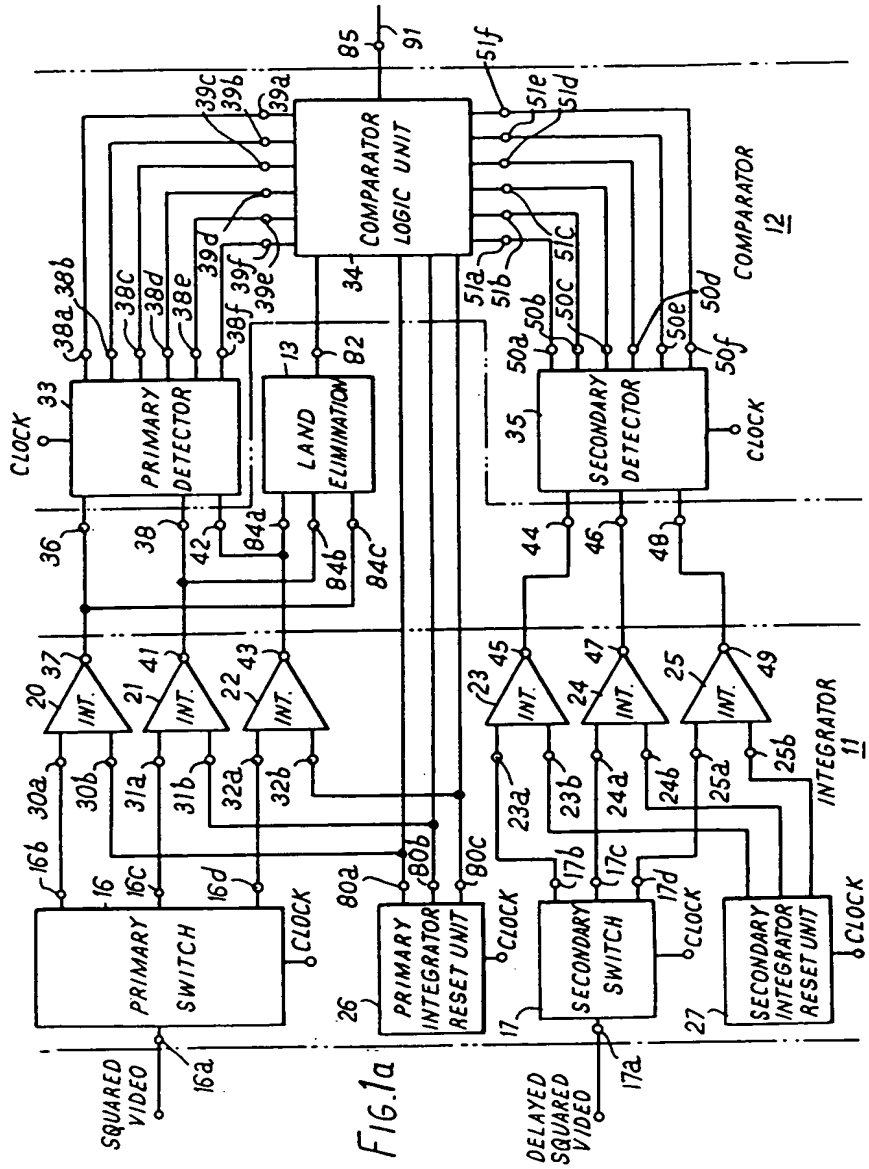

FIG. 1a

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Sheet 2

FIG. 1b

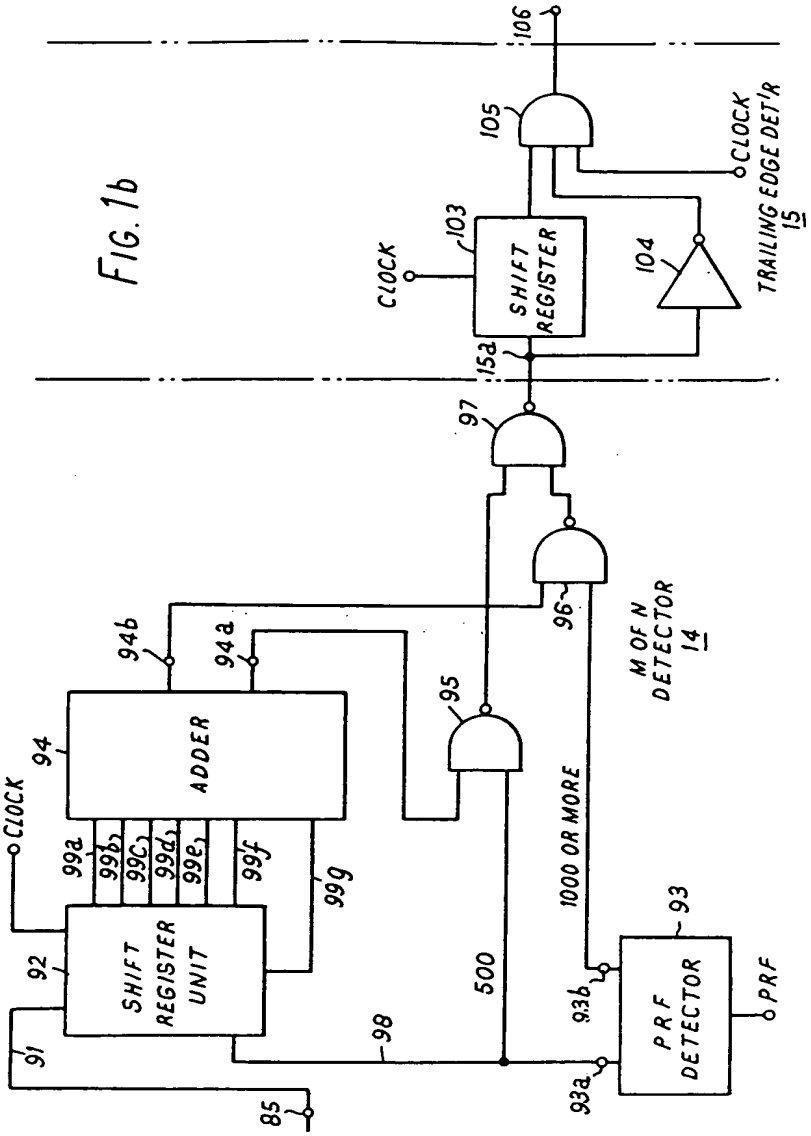

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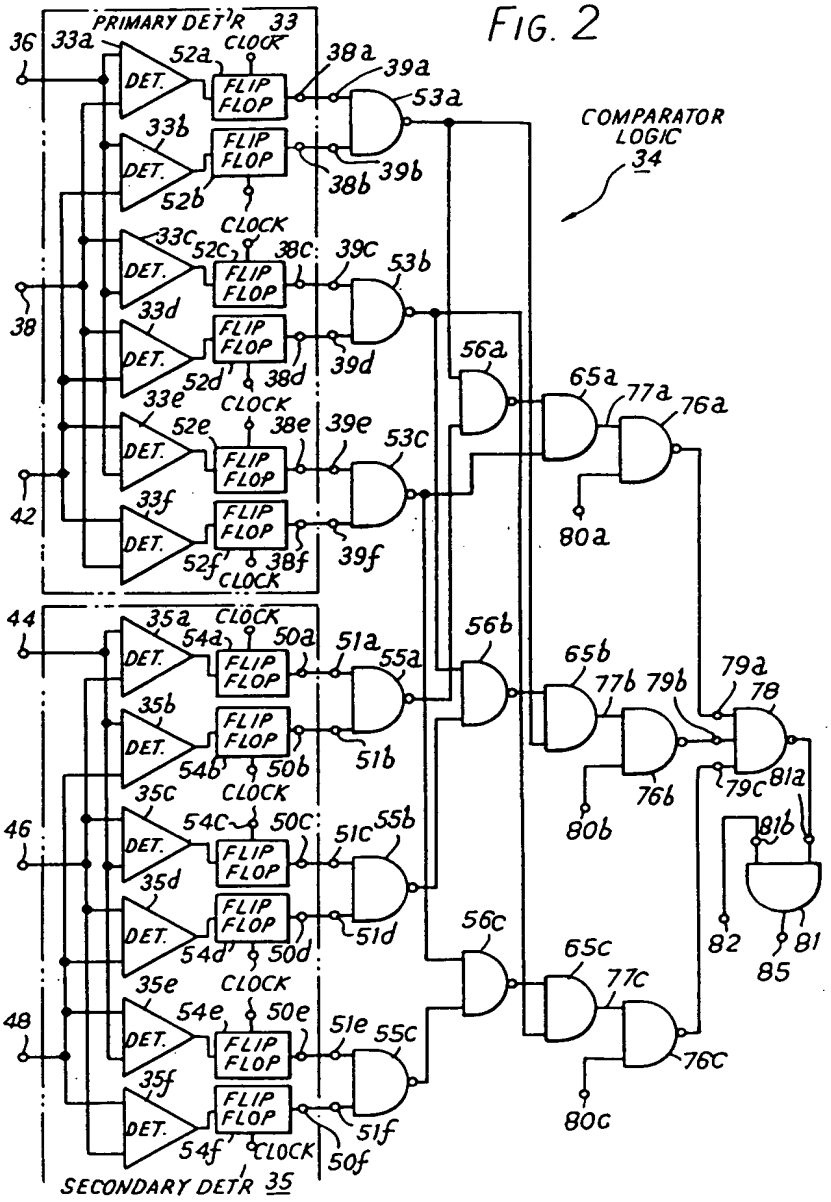
FIG. 2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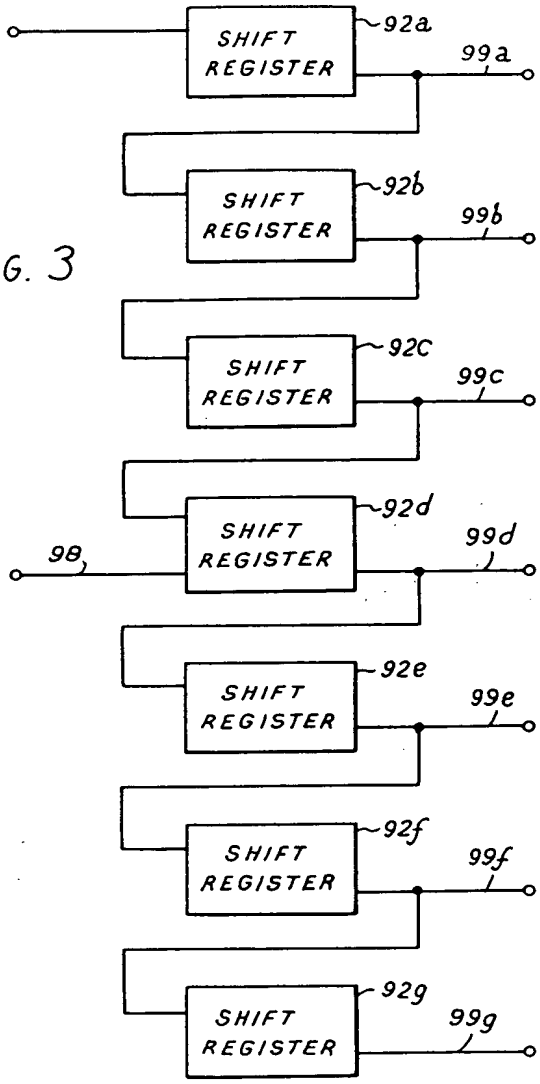
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FIG. 3

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